What is claimed is:

1. A method of writing date to a memory device comprising a plurality of memory cells, wherein each memory cell comprises a latch circuit having first and second complementary latch outputs and first and second write circuits respectively coupled to said first and second latch outputs, the method comprising:

selecting a memory cell to which data is to be written;

activating a write word line coupled to the first and second write circuits of the selected memory cell to which data is to be written;

applying complementary write values to complementary write bit lines of a write bit line pair coupled with the first and second write circuits of the selected memory cell; and

responsive to activating the write word line coupled to the first and second write circuits of the selected memory cell to which data is to be written, coupling the first and second latch outputs of the selected memory cell with the complementary write bit lines of the write bit line pair coupled therewith to write the complementary write values to the first and second latch outputs of the selected memory cell.

2. A method according to Claim 1 wherein the memory device comprises a plurality of complementary write bit line pairs with bit lines of each pair respectively coupled with first and second write circuits of pluralities of memory cells wherein bit lines of bit line pairs not coupled with the selected memory cell are set at a same value.

3. A method according to Claim 2 wherein the bit lines of the complementary write bit line pairs not coupled with the selected memory cell are set at a same high logic value.

4. A method according to Claim 1 further comprising:

generating a control signal on a control line coupled to a plurality of the memory cells; and

responsive to generating the control signal, resetting all of the plurality of the memory cells to a same reset condition.

5. A method according to Claim 4 wherein the memory device comprises a plurality of control lines each coupled to a different plurality of memory cells.

6. A memory device comprising:

a plurality of memory cells wherein each memory cell comprises a latch circuit having first and second complementary latch outputs and first and second write circuits respectively coupled to said first and second latch outputs;

a plurality of write word lines wherein each write word line is coupled with the first and second write circuits of a respective plurality of memory cells;

a plurality of complimentary write bit line pairs wherein write bit lines of each complimentary write bit line pair are respectively coupled with the first and second write circuits of a plurality of memory cells; and

a controller that selects a memory cell to which data is to be written, activates a write word line coupled to the first and second write circuits of the selected memory cell to which data is to be written, and applies complementary write values to complementary write bit lines of a write bit line pair coupled with the first and second write circuits of the selected memory cell, so that the first and second latch outputs of the selected memory cell are coupled with the complementary write bit lines of the write bit line pair coupled therewith to write the complementary write values to the first and second latch outputs of the selected memory cell responsive to activating the write word line coupled to the first and second write circuits of the selected memory cell.

7. A memory device according to Claim 6 wherein the controller applies a same value to complementary bit lines of complementary bit line pairs not coupled with the selected memory cell.

8. A memory device according to Claim 7 wherein the controller applies a

same high logic value to complementary write bit lines of the complementary write bit line pairs not coupled with the selected memory cell.

9. A memory device according to Claim 6 wherein each memory cell comprises a set/reset circuit, the memory device further comprising:

a plurality of control lines wherein each control line is coupled to set/reset circuits of a respective plurality of memory cells and wherein the set/reset circuits coupled to a control line reset the respective memory cells to a same set/reset condition responsive to a control signal on the respective control line.

10. A memory device according to Claim 6 wherein the latch circuit of each memory cell is coupled to a read circuit, the memory device further comprising:

a plurality of virtual ground lines wherein each virtual ground line is coupled with read circuits of a respective plurality of memory cells; and

wherein the controller selects a memory cell from which data is to be read, applies a first reference voltage to a virtual ground line coupled to the selected memory cell from which data is to be read, applies a second reference voltage to a virtual ground line not coupled to the selected memory cell, and activates a read word line coupled to the read circuit of the selected memory cell from which data is to be read, so that data is coupled from the latch circuit of the selected memory cell with a respective read bit line through the read circuit of the selected memory cell responsive to activating the read word line coupled to the read circuit of the selected memory cell.

11. A memory device comprising:

a plurality of write word lines;

a plurality of complementary write bit line pairs; and

a plurality of memory cells wherein each memory cell comprises a latch circuit that latches first and second complementary logic values at first and second outputs thereof, a first write circuit coupled between the first latch output and a first write bit line of a complimentary write bit line pair coupled to the memory cell, and a second

write circuit coupled between the second latch output and a second write bit line of the complimentary write bit line pair coupled to the memory cell, so that the first and second latch outputs are coupled to the respective first and second write bit lines of the complementary write bit line pair coupled to the memory cell responsive to a write signal on the write word line coupled with the memory cell.

12. A memory device according to Claim 11 wherein the first write circuit of a memory cell comprises a first transistor having a first source/drain coupled to the first latch output, a second source/drain coupled to the first write bit line of the complementary write bit line pair, and a gate coupled to the write word line, and wherein the second write circuit of the memory cell comprises a second transistor having a third source/drain coupled to the second latch output, a fourth source/drain coupled to the second write bit line of the complementary write bit line pair, and a gate coupled to the write word line.

13. A semiconductor memory cell of a plurality of semiconductor memory cells that are arranged in a column direction and a row direction in a semiconductor memory device, the semiconductor memory cell comprising:

at least one write word line;

at least one write bit line;

at least one read word line;

at least one read bit line;

at least one virtual ground;

a latch circuit for latching a predetermined voltage and including first and second nodes having opposite voltage levels;

a first write circuit for transmitting a first external voltage loaded in a first write bit line of the at least one write bit line to the first node in response to a signal of a first write word line of the at least one write word line; and

a read circuit for inverting the voltage level of the second node in response to a signal of a first read word line of the at least one read word line and in response to

the at least one virtual ground and transmitting the voltage to a first read bit line of the at least one read bit line;

wherein the virtual ground latches a first voltage in a case where the virtual ground is connected to a semiconductor memory cell selected from the plurality of semiconductor memory cells, and the virtual ground latches a second voltage, which is logically opposite to the first voltage, in a case where the virtual ground is connected to an unselected semiconductor memory cell.

14. The semiconductor memory cell as claimed in claim 13, wherein the first voltage is a ground voltage, and the second voltage is a supply voltage.

15. The semiconductor memory cell as claimed in claim 13, wherein the first write circuit includes a first NMOS transistor, which has one end connected to the first write bit line, and another end connected to the first node, and a gate connected to the first write word line.

16. The semiconductor memory cell as claimed in claim 13, wherein the read circuit comprises;

a second NMOS transistor, which has one end connected to the first read bit line and a gate connected to the first read word line; and

a third NMOS transistor, which has one end connected to the other end of the second NMOS transistor, another end connected to a first virtual ground, and a gate connected to the second node.

17. The semiconductor memory cell as claimed in claim 13, further comprising a second write circuit for transmitting second external voltage loaded in a second write bit line of the at least one write bit line to the second node in response to the first write word line, wherein the first external voltage and the second external voltage have logically opposite voltage levels.

18. The semiconductor memory cell as claimed in claim 17, wherein the

second write circuit includes a fourth NMOS transistor, which has one end connected to the second node, another end connected to the second write bit line, and a gate connected to the write word line.

19. The semiconductor memory cell as claimed in claim 13, further comprising a set circuit for setting the first node.

20. The semiconductor memory cell as claimed in claim 13, further comprising a reset circuit for resetting the second node.

21. The semiconductor memory cell as claimed in claim 13, wherein the read circuit further comprises:

a fifth NMOS transistor, which has one end connected to a second read bit line of the at least one read bit line and a gate connected to a second read word line of the at least one read word line; and

a sixth NMOS transistor, which has one end connected to the other end of the fifth NMOS transistor, another end connected to a second virtual ground, and a gate connected to the second node.

22. A semiconductor memory cell comprising:

a write word line;

a write bit line;

a read word line;

a read bit line;

a virtual ground;

a latch circuit for latching a predetermined voltage and including first and second nodes having opposite voltage levels;

a write circuit for transmitting a first external voltage loaded in the write bit line to the first node in response to a signal of the write word line; and

a read circuit for inverting the voltage level of the second node in response to a signal of the read word line and the virtual ground and transmitting the voltage to

the read bit line,

wherein the virtual ground is ground voltage or a supply voltage which can be changed.